ABSTRACT OF THE DISCLOSURE

A nonvolatile semiconductor memory device having a small layout area includes a memory cell array in which a plurality of memory cells are arranged in a row direction and a column direction. The memory cell array includes source line diffusion layers, each of the source line diffusion layers extending along the row direction and connecting in common with the memory cells arranged in the row direction, bitline diffusion layers, element isolation regions which separate each of the bitline diffusion layers, and word gate common connection sections. Each of the memory cells includes a word gate and a select gate. One of the bitline diffusion layers is formed between two word gates adjacent in the column direction Y. Each of the word gate common connection sections is connected with the two word gates above one of the element isolation regions.